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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,722	01/23/2002	Akio Kitamura	FUJI:203	6219

7590 05/05/2003

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EXAMINER
FENTY, JESSE A

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 05/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,722	KITAMURA, AKIO	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-8 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al (U.S. Patent No. 5,541,125) in view of Krivokapic et al. (U.S. Patent No. 6,238,982 B1).

In re claim 1, Williams discloses a semiconductor device, comprising:

A semiconductor substrate (10);

A first later MOS transistor (16V NMOS) and a second lateral MOS transistor (20V NMOS) integrated in the semiconductor substrate, wherein said first MOS transistor has a smaller channel length than said second MOS transistor; and

A punch-through stopper area (P-Well) that surrounds a source area and a drain are of said first MOS transistor and provides a punch-through voltage resistance between said source area and said drain area.

Williams does not expressly disclose the second lateral MOS transistor having a threshold voltage lower than the first lateral MOS transistor. Krivokapic discloses techniques for varying the threshold voltage of lateral MOS transistors such as varying the gate length and doping the channel region (column 5, lines 15-20, 51-66). It would have been obvious to one

skilled in the art at the time of the invention to further vary the threshold voltages of the lateral MOS transistors disclosed by Williams in a manner disclosed by Krivokapic for the purpose of creating a more diverse integrated circuit structure.

In re claim 2, Williams in view of Krivokapic discloses the device of claim 1. The distinction between the first and second MOS transistors composing digital and analog devices respectively are recitations of the intended use of the claimed device. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art.

In re claim 3, Williams in view of Krivokapic discloses the device of claim 1, wherein a drain area (152) of said second MOS transistor is surrounded by an offset drain area (122) having a lower impurity concentration than the drain are of the second MOS transistor.

In re claim 4, Williams in view of Krivokapic discloses the device of claim 3, further comprising a punch-through stopper area (corresponding 122) that surrounds a source area (corresponding 152) of said second MOS transistor and provides a punch-through voltage resistance between the source area of said second MOS transistor and said offset drain area.

In re claim 5, Williams in view of Krivokapic discloses the device of claim 1, further comprising a bipolar transistor integrated in said semiconductor substrate.

In re claim 6, Williams in view of Krivokapic discloses the device of claim 1, further comprising a diode (there are many PN junction-diodes in the device) integrated in said semiconductor substrate.

In re claim 7, Williams in view of Krivokapic discloses the device of claim 1, further comprising a diffusion resistor integrated in said semiconductor substrate.

In re claim 8, Williams in view of Krivokapic discloses the device of claim 1, wherein said source area includes a source LDD area and said drain area includes a drain side LDD area, and wherein the punch-through stopper area (P-well) has a pocket structure and at encloses the source side LDD area and the drain side LDD area.

In re claim 11, Williams in view of Krivokapic discloses the device of claim 1, further including a well (40) having a lower impurity concentration than that of the puch-through stopper region formed in the substrate, wherein the punch-through stopper area is formed in the well.

Response to Arguments

3. Applicant's arguments filed 02/14/03 have been fully considered but they are not persuasive.

Applicant argues that Williams does not disclose or teach a second MOS transistor having a larger channel length than a first channel. The transistor with the larger channel length is the 20V DMOS. Incidentally, while "DMOS" sometimes refers to a vertical transistor; in this instance, the 20V DMOS is lateral. The "D" simply relates to the "double diffused" source/drain regions (122, 152).

Second, the Krivokapic is more or less used as a teaching reference to show how threshold voltages may be varied in a transistor device. That the threshold voltages of Williams may be varied by the methods disclosed by Krivokapic mirrors the disclosure of the instant application. On pages 7 and 9 of the instant application, applicant teaches that the threshold voltages "can be set at a low value" by use of the punch-through region. By the same token, the

device of Williams, disclosing channel lengths of varying lengths similar to the applicant, can have the threshold voltage of each of the transistors varied by means known in the art, for example by varying the dopant concentration of the channel.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 703-308-8137. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-308-1690. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-746-3892 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Jesse A. Fenty
Examiner
Art Unit 2815

JAF
May 1, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800